Understanding Simultaneous Impact of Network QoS and Power on HPC Application Performance

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Abstract—**With the growing complexity of high performance computing (HPC) systems, application performance variation has increased enough to disrupt the overall throughput of the systems. Such performance variation is expected to worsen in the future, when job schedulers will have to manage *flow* resources such as power, network and I/O in addition to traditional resources such as nodes and memory. In this work, we study the simultaneous impact of inter-job interference, Infiniband service levels, and power capping on different applications in a controlled experimental setup, with the goal of understanding the range of performance variation as well as potential mitigation strategies.**

I. INTRODUCTION

Performance variation and unpredictability in modern supercomputers are growing concerns. On current HPC systems, user applications already experience about 20% run-to-run variation with the exact same input configuration [3]. Such variation is typically attributed to *interference from neighboring jobs* or to manufacturing differences on power-limited systems [5]. Limited understanding of the sources of run-to-run variation and the range of variation can reduce the overall efficiency of the system. As we venture toward exascale, scientific reproducibility will worsen if system software (such as job scheduler) does not adapt to the changing landscape of managing *flow resources* such as network bandwidth and power *simultaneously*.
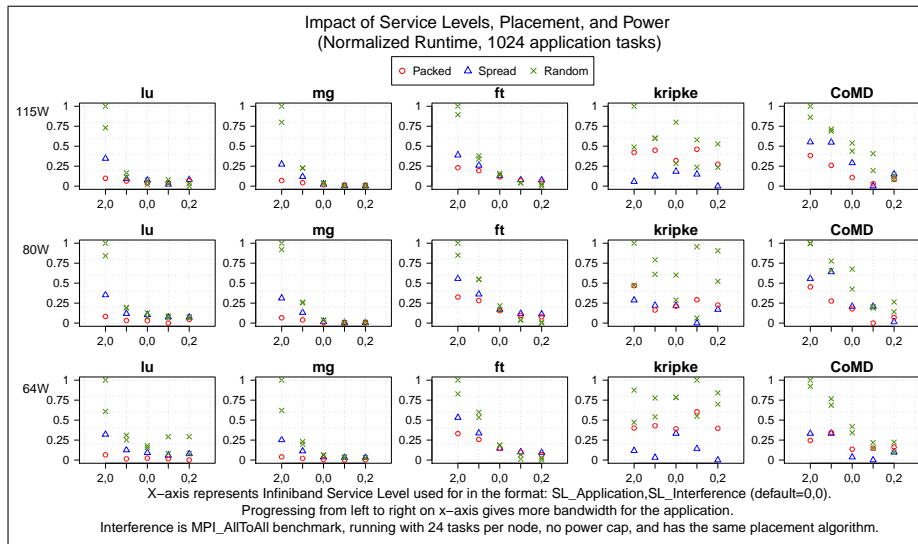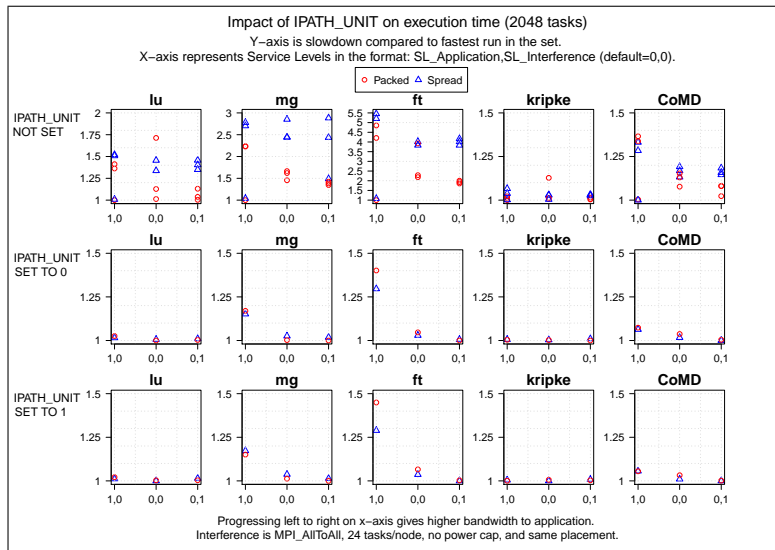
Most modern schedulers do not consider flow resources when making allocation decisions, even though it has been shown that there is tremendous scope for improving throughput and utilization [9], [10]. One of the primary reasons for this is the lack of understanding of application performance variation and its sources. For system schedulers to be able to boost throughput, both application performance and the associated range of run-to-run variation need to be predictable to some degree. Our goal is to construct a dataset of application performance subject to changing parameters such as power, network bandwidth, and rank-to-node mapping/placement. Such a dataset can be used to create effective performance prediction models, which can then be used for future scheduling research. Creating this dataset is extremely challenging because scheduling environments are dynamic in nature. Therefore, in this work, we run simpler *control jobs* that can be well understood when subject to different parameters instead of complex applications.

II. EXPERIMENTAL METHODOLOGY AND RESULTS

We run our experiments on the `catalyst` cluster, which is located at Lawrence Livermore National Laboratory. Catalyst is a 150 TeraFLOP/s, 324-node cluster with two 12-core Intel Xeon CPUs per node. Catalyst has an InfiniBand QDR network with a two-level fat-tree topology. Each node has two HCA network adapters, and there are 18 nodes per switch (total 18 switches). For power-capping, we use Intel's RAPL technology which is supported through `libmsr` [8] and `msr-safe`. The range for CPU power capping is between 65W and 115W. For controlling the network QoS, we use the `IPATH_SL` environment variable to select the virtual lanes [4]. 4 service levels associated with 4 virtual lanes are available (0 being the highest bandwidth, and 3 being the lowest bandwidth). The default setting is to run at service level 0 and the maximum CPU power of 115W. The *control jobs* we use are LU, FT and MG from NAS [2], and the Kripke and CoMD proxy applications [6], [7]. We generate inter-job interference by using the OSU `MPI_Alltoall` benchmark [1] using 32KB messages. We use 256-node allocations for our experiments, which is split between the control job and the interfering job. We pick three placement algorithms: `packed`, `spread` and `random`. Packed places all application ranks as close together as possible, so that the fewest number of switches are used from the fat tree. Spread distributes the ranks in a round-robin manner across the switches.

Figures 1 and 2 show our data[1]. Figure 1 shows the impact of using both the network adapters as opposed to picking one adapter across 5 benchmarks (2048 application ranks/86 nodes). Setting `IPATH_UNIT` selects one of the two adapters, and more bandwidth is allocated to the application (and less to interference) as we progress from left to right on the x-axis. Our main counter-intuitive observation here is the significant amount of variation that we see when both adapters are used, which is the default configuration on most HPC clusters. Note the scale of the y-axis, over 5x run-to-run variation was observed in our simple control benchmarks (e.g. FT). This can be mitigated by choosing one of the two adapters (see rows 2 and 3). In Figure 2, we set the IPATH_UNIT to 0, and further explore power capping and additional service levels. Here, we make three key observations: (1) contrary to popular belief of topology-aware scheduling, applications benefit from being spread across the switches (e.g. Kripke), (2) the default service

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[1]More details and data can be made available in a full paper

Impact of IPATH_UNIT on execution time (2048 tasks)
Y–axis is slowdown compared to fastest run in the set.
X–axis represents Service Levels in the format: SL_Application,SL_Interference (default=0,0).

Progressing left to right on x–axis gives higher bandwidth to application.
Interference is MPI_AllToAll, 24 tasks/node, no power cap, and same placement.

Impact of Service Levels, Placement, and Power
(Normalized Runtime, 1024 application tasks)

X–axis represents Infiniband Service Level used for in the format: SL_Application,SL_Interference (default=0,0).
Progressing from left to right on x–axis gives more bandwidth for the application.
Interference is MPI_AllToAll benchmark, running with 24 tasks per node, no power cap, and has the same placement algorithm.

level of zero can result in poor performance, and there are scenarios where running the application at a lower service level (with low-bandwidth) but with no interference turns out to be better; and (3) different placement algorithms may be needed based on the power cap under consideration. Our next step is to explore prediction models and algorithms for advanced research of HPC system software with such data.

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